

Application Serial No. 10/615,708
Reply to Office Action of March 23, 2005

PATENT
Docket: CU-3283

Amendments To The Abstract

Marked-up Version

The following marked-up version of the amended Abstract is attached hereto to aid the Examiner in identifying the changes:

~~The present invention relates to a method for fabricating a semiconductor device, which comprises the steps of: forming a device isolation film defining a device region in a silicon substrate; depositing a conductive layer on the substrate and patterning the deposited conductive layer so as to form a gate electrode on the substrate; implanting impurity ions into the substrate so as to form junction regions in the substrate; forming an interlayer insulating film on the substrate and selectively patterning the interlayer insulating film so as to partially expose the surface of the substrate;~~

In a silicon substrate having a contact hole in a device region, the contact resistance between the contact plug and the silicon substrate is reduced by preventing formation of the unwanted layer therebetween by treating the exposed surface of the substrate before forming the contact plug.
~~;~~ and forming Further, a two-layered contact plug consisting of a first contact plug layer having high impurity concentration and a second contact plug layer having low impurity concentration, on the interlayer insulating film including the exposed surface of the substrate. ~~According to the present invention, the~~ The interface between the silicon substrate and the contact plug is thermally treated at low temperature, and the first contact plug layer having high impurity concentration and the second contact plug layer having low impurity

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concentration, are formed, so that the resistance between the silicon substrate and the contact plug can be reduced, thereby increasing the operation speed of the device.

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REMARKS/ARGUMENTS

Reconsideration is respectfully requested.

As to the objection to the Abstract, the new Abstract for replacement is attached hereto, and withdrawal of the objection is respectfully requested.

Claims 1-19 are pending in the present application before this amendment. By the present amendment, Claim 7 has been cancelled without prejudice. Claims 1, 9, and 13 have been amended. No new matter has been added.

Claims 1 and 13 stand objected to for containing informalities. Examiner's suggested amendments have been made to Claim 1, and Claim 13 has been cancelled. Withdrawal of the objection is respectfully requested.

Claim 9 is objected to for bearing improper dependency. Claim 9 has been amended to depend from Claim 8, and withdrawal of the objection is respectfully requested.

Claims 1, 7, 13, and 16 stand rejected under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,792,695 (Ono) in view of U.S. Patent No. 5,681,770 (Ogura). The "et al." suffix, which may appear after a reference name, is omitted in this paper.

Applicants respectfully disagree.

Claim 1, as amended, recites, inter alia, the following limitation that is not taught or suggested by Ono, Ogura, Lin, Anderson, and other cited references, whether they are considered individually or in combination:

—forming a two-layered contact plug consisting of a first contact layer of **monocrystalline silicon** grown on the interlayer insulating film including the exposed surface of the substrate at a temperature **less than 700 degrees**

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Celsius and a second contact layer of polycrystalline silicon on the first contact layer--

One of many problems of the prior art that are solved by the presently claimed invention is that the resistance between the contact plug material and the silicon substrate is rather high (in the magnitude of about 10K Ohms, and this is known to be due to the formation of "native oxides" and "carbon-containing residues" at the interface between the contact plug and the silicon substrate (the Specification, Background, page 2, lines 10-18).

This type of undesirable layer that causes high resistance are very related to the conventional or prior art method of fabrication as described in the Specification page 2, line 19 to page 4, line 2.

In prior art, impurity doped polycrystalline silicon material is used to form a contact plug (Specification page 1, line 24). In prior art, the process to form the polycrystalline based contact plug is performed almost immediately after a wet cleaning process of the surface; however, the prior art technique **still cannot prevent** the formation of the unwanted native oxide layer (Specification page 2, lines 19-24).

The prior art may also teach cleaning the silicon substrate with non-organic volatile compound solution and de-ionized water (Specification page 3, lines 1-3); however, this still is ineffective to prevent the unwanted oxide layer.

Yet further, the prior art may also teach selective epitaxial growth (SEG) of silicon by LPCVD utilizing, for example, reaction gases at a temperature higher than 800 degrees Celsius (Specification page 3, lines 7-16). Further, before performing the SEG, the silicon substrate is treated with H₂ at a temperature higher than 800 degrees Celsius

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(Specification page 3, lines 22-24). But the high temperature involved here causes problems in deteriorating the device characteristics.

The presently claimed invention solves all of the above prior art problems. That is the presently claimed invention provides solutions that will (1) reduce the resistance between the silicon substrate and a contact plug (Specification page 1, lines 9-10) but (2) without adversely affecting the device characteristics by not subjecting to the high temperature process of the prior art.

That is, the presently claimed invention teaches, inter alia, a two-layer structure contact plug. In forming a contact plug, a monocrystalline silicon having low contact resistance is grown first at the lowest possible temperature of less than 700 degrees Celsius (Specification page 3, lines 19-22; page 7, lines 5-10), then a polycrystalline silicon is grown (Specification page 10, lines 10-12).

Accordingly, Claim 1 and 13 have been amended to include this novel feature of the present invention.

None of the cited prior art references (considered individually or in any combination) teaches Claim 1, as amended.

As to Ono, the layers 16 and 17 cited (see col. 6, lines 10-67) are all doped "polysilicon" layers.

As to Hsu, the layer 212 is also a doped polysilicon layer (col. 4, lines 53-63) and the layer 224 is a tungsten layer. Likewise, the layer 312 is also a doped polysilicon layer (col. 4, lines 30-40) and the layer 320 is a silicon nitride layer (col. 6, lines 40-45).

All other cited references, including Ogura, Nakaiima, Lin and others, fails to show the claimed contact plug structure of two layer.

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Importantly, it is noted that silicon exists in three different forms: monocrystalline silicon; polycrystalline silicon; and amorphous silicon. Atoms in the polycrystalline silicon are spatially arranged in a periodic fashion, but the polycrystalline silicon is made up of small crystal grains, the size of which affect the electronic property of the polycrystalline material. On the other hand, the monocrystalline silicon is formed by the periodic arrangement of the atoms throughout the entire solid. Generally, it is known that monocrystalline silicon has a very low resistance to electron flow. (Amorphous silicon has atoms or ions that are arranged randomly and consists of dangling bonds and voids.)

Accordingly, it is respectfully submitted that Claim 1, as amended, is not taught or suggested by any of the cited references (individually or in combination). Accordingly, indication of allowability of Claim 1 is respectfully requested.

Claims 2-6 and 14-15 stand rejected under 35 U.S.C. § 103(a) as being obvious over Ono in view of Ogura, and further in view of U.S. Patent No. 6,100,202 (Lin). Claims 8-12 and 17-19 stand rejected under 35 U.S.C. § 103(a) as being obvious over Ono in view of Ogura, and further in view of U.S. Patent No. 5,916,369 (Anderson).

Claims 2-19 are considered to be allowable at least since they depend from Claim 1, which is considered to be allowable for the reasons above.


For the reasons set forth above, Applicants respectfully submit that Claims 1-19, pending in this application, are in condition for allowance over the cited references. This amendment is considered to be responsive to all points raised in the Office Action. Accordingly, Applicants respectfully request reconsideration and withdrawal of the outstanding rejections and earnestly solicit an indication of allowable subject matter.

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Should the Examiner have any remaining questions or concerns, the Examiner is encouraged to contact the undersigned attorney by telephone to expeditiously resolve such concerns.

Respectfully submitted,



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